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High Performance Multi-Level Non-Volatile Polymer Memory with Solution-Blended Ferroelectric Polymer/High-*k* Insulators for Low Voltage Operation

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Polymer ferroelectric-gate field effect transistors (Fe-FETs) employing ferroelectric polymer thin films as gate insulators are highly attractive as a next-generation non-volatile memory. Furthermore, polymer Fe-FETs have been recently of interest owing to their capability of storing data in more than 2 states in a single device, that is, they have multi-level cell (MLC) operation potential for high density data storage. However, among a variety of technological issues of MLC polymer Fe-FETs, the requirement of high voltage for cell operation is one of the most urgent problems. Here, a low voltage operating MLC polymer Fe-FET memory with a high dielectric constant (*k*) ferroelectric polymer insulator is presented. Effective enhancement of capacitance of the ferroelectric gate insulator layer is achieved by a simple binary solution-blend of a ferroelectric poly(vinylidene fluoride-co-trifluoroethylene) (PVDF-TrFE) (*k* ≈ 8) with a relaxer high-*k* poly(vinylidene-fluoride–trifluoroethylene–chlorotrifluoroethylene) (PVDF-TrFE-CTFE) (*k* ≈ 18). At optimized conditions, a ferroelectric insulator with a PVDF-TrFE/PVDF-TrFE-CTFE (10/5) blend composition enables the discrete six-level multi-state operation of a MLC Fe-FET at a gate voltage sweep of ±18 V with excellent data retention and endurance of each state of more than 10^4 s and 120 cycles, respectively.

1. Introduction

Ferroelectric-gate field effect transistors (Fe-FETs) employing ferroelectric thin films as gate insulators are greatly attractive as a next generation non-volatile memory because of their various advantages including a non-destructive readout capability and scalable feature size of $4F^2$.[1] In particular, due to the variety of additional benefits of ferroelectric polymers such as low cost, compatibility with solution-based processes, and mechanical flexibility, great efforts have been devoted to improve the memory performance of Fe-FETs using ferroelectric polymers such as poly(vinylidene fluoride) (PVDF),[2] poly(vinylidene fluoride-chlorotrifluoro ethylene) (PVDF-CTFE),[3] and poly(vinylidene fluoride-co-trifluoroethylene) (PVDF-TrFE).[4–10] The polarization switching of these fluorine-based ferroelectric polymers is accomplished by facile rotation of the permanent dipole between hydrogen and fluorine atoms, which controls accumulation or depletion of carriers in the semiconducting channel between the source and drain electrodes.

Polymer Fe-FETs have also attracted much attention owing to their ability to store data of more than 2 states in a single device, that is, multi-level cell (MLC) operation.[11–14] The distributed domain polarization of a ferroelectric layer controlled by the applied gate voltage precisely defines the discrete interstate levels of the source-drain current, giving rise to a MLC Fe-FET with highly reliable data retention and read/write endurance cycle performance compared with other organic or polymer-based non-volatile memory.[15] The MLC operation is extremely important, especially for polymer non-volatile memories, most of which are fabricated by printing technologies hardly applicable for the high definition, nanometer scale pattern formation necessary for high density data storage devices.

Among a variety of technological issues that limit the performance of multilevel polymer Fe-FETs, the requirement of high voltage for cell operation is one of the most urgent problems that still remains unresolved. Most bistable, 1-bit (program/erase) polymer Fe-FETs require a gate voltage greater than 50 V due to the use of thick ferroelectric gate insulators to minimize the electrical leakage arising from many structural defects, including grain boundaries of semi-crystalline polymers, pinholes, and residual solvent trapped in the film.[10,16,17] In fact, our MLC Fe-FET with a top gate/bottom contact device architecture also required a voltage of 80 V for full operation of 4 different levels.[15]

The previous strategy to reduce the leakage current of a thin PVDF-TrFE film and, at the same time, reduce the operating voltage of a Fe-FET was to employ a thin electrically insulating interlayer between the gate electrode and the ferroelectric layer while maintaining a high capacitance. Although various interlayers were examined including SiO_2,[18] Al_2O_3,[19,20] HfTaO,[21] PVP,[2,22,23] and a random copolymer of polystyrene and poly(methylmethacrylate)(P(S-r-MMA)),[24] the results were not

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very successful. More importantly, most of these layers were not suitable for top gate Fe-FETs, which are more beneficial for reliable multi-state operation due to a high memory margin from the auto-encapsulation of air-sensitive organic semiconductors by the overlaid gate insulator and electrode.[25] One way to address the high operation voltage issue of a MLC Fe-FET is to fabricate a relatively thick and electrically robust PVDF-TrFE film homogeneously mixed with high-k materials. The enhancement of capacitance of these types of hybrid films with the high dielectric constant (k) materials can allow a decrease in operation voltage of a MLC Fe-FET even with a sufficiently thick ferroelectric polymer insulator that minimizes gate leakage current and thus ensures a low OFF state source-drain current, giving rise to a MLC device with clearly distinguishable current levels. Furthermore, the approach of blending high-k materials with a ferroelectric polymer is advantageous because it offers a facile platform to control the operation voltage of a MLC Fe-FET as a function of the amount of high-k materials.

In this paper, we present a simple but robust route to fabricate a low voltage operating MLC polymer Fe-FET memory with top gate/bottom contact architecture. Our method is based on precise control of capacitance of a ferroelectric gate insulator layer by solution-blending a ferroelectric polymer with high-k materials. Binary blending of PVDF-TrFE ($k \approx 8$) and poly(vinylidene-fluoride–trifluoroethylene–chlorotrifluoroethylene) (PVDF-TrFE-CTFE) ($k \approx 18$) enabled us to control the capacitance of the films ranging from 9 to 13 without significant deterioration of ferroelectric switching characteristics of PVDF-TrFE. The enhancement of capacitance of a ferroelectric hybrid film successfully led to the reduction of operation voltage of MLC Fe-FET memory when the insulator was employed in a Fe-FET device. For instance, a hybrid insulator with a PVDF-TrFE/PVDF-TrFE-CTFE blend composition of 10/5 allowed discrete six-level multi-state operation of a MLC Fe-FET at a gate voltage sweep of 18 V with excellent data retention and endurance of each state of more than 10^4 s and 120 cycles, respectively.

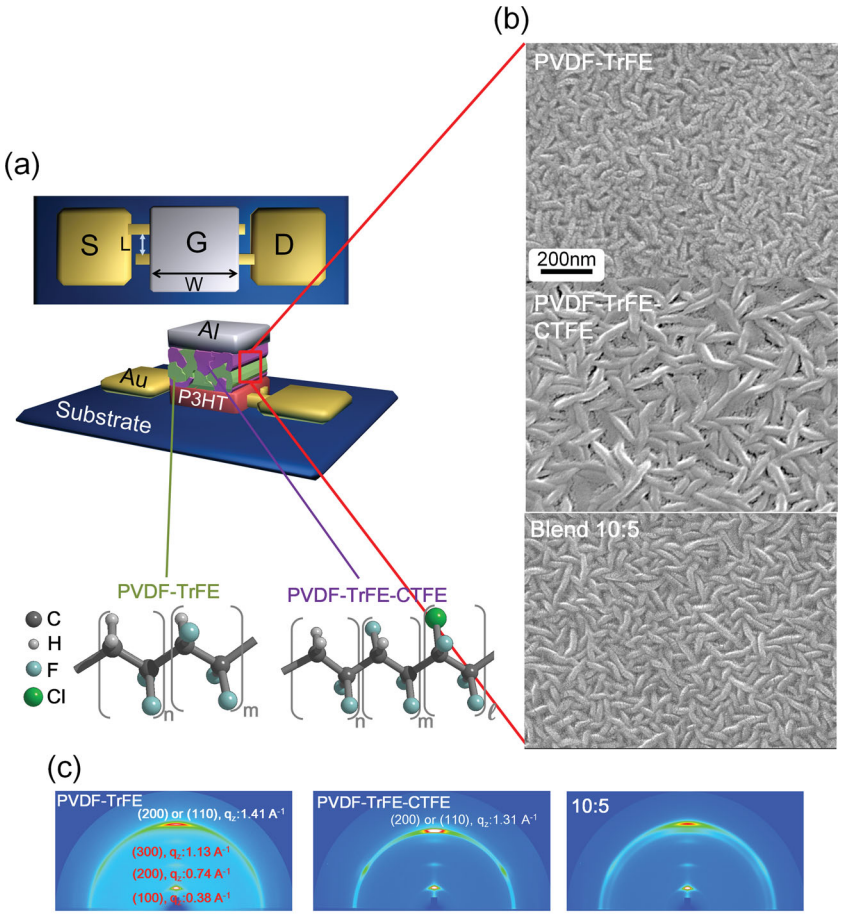

Figure 1. a) Schematic of the TGBC Fe-FET memory device with a P3HT channel and solution-blended ferroelectric insulator. b) Plane view SEM images of the blended ferroelectric films with PVDF-TrFE:PVDF-TrFE-CTFE compositions of 10:0, 0:10, and 10:5. c) 2D GIWAXS patterns of PVDF-TrFE, PVDF-TrFE-CTFE, and a blended polymer film spin-coated and subsequently annealed at 135 °C on a P3HT layer.

2. Results and Discussion

A Fe-FET memory device with a top-gate bottom-contact (TGBC) structure consists of a Au source-drain (S/D) electrode/poly(3-hexylthiophene) (P3HT)/blended ferroelectric film/Al gate electrode sequentially constructed on a Si substrate, as schematically illustrated in **Figure 1**a. A 50-nm-thick P3HT layer was directly spin-coated onto the patterned Au S/D electrodes from a solution in 1,2-dichlorobenzene. Subsequently, a PVDF-TrFE/PVDF-TrFE-CTFE blend film (3.5 wt% in methyl ethyl ketone, MEK) with various mixing compositions was prepared by spin-coating onto the P3HT layer and annealing at 135 °C for 2 h, followed by thermal evaporation of the Al gate electrodes through a shadow mask. The blended ferroelectric films with different compositions were all similar in thickness of approximately 350 nm (Supporting Information, Figure S1). Finally, to isolate the two cells as well as to make the Au S/D electrode accessible to contact probes, both the P3HT and ferroelectric films in the regions outside the areas covered by the top Al electrodes were etched by oxygen plasma using reactive ion etching (RIE), completing the fabrication of the Fe-FET device.

The molecular and microstructures of the PVDF-TrFE/PVDF-TrFE-CTFE blend films on a P3HT layer were visualized by field emission scanning electron microscopy (FESEM) and two-dimensional grazing-incidence wide-angle X-ray scattering (GIWAXS). Figure 1b shows the morphologies of thin films of PVDF-TrFE, PVDF-TrFE-CTFE, and a 10:5 blend on a P3HT layer. Although all the films exhibited the characteristic randomly distributed needle-like shape microdomains, the

microdomains of PVDF-TrFE-CTFE were larger in size than those of PVDF-TrFE due to the slower crystallization kinetics of the terpolymer. When the two polymers were mixed in a blended film, the crystallization kinetics of both polymers averaged, resulting in microdomains whose size was between those of the pure components, as shown in Figure 1b (also see Supporting Information, Figure S2).

The 2D GIWAXS patterns of pure PVDF-TrFE and PVDF-TrFE-CTFE annealed at 135 °C are shown in Figure 1c. These patterns display an intensified reflection at a scattering vector, q_z, of approximately 1.41 Å^{-1} and 1.31 Å^{-1}, respectively, arising for both polymers from either the (110) or (200) plane of an orthorhombic crystal cell in which the similar lattice spacing of (110) and (200) gives rise to a pseudo-hexagonal diffraction pattern.[26,27] Both diffraction patterns also show multiple, high-order reflections where q_z is approximately 0.38, 0.74, and 1.13 Å^{-1} at the meridian, which corresponds to the (00l) plane of the P3HT crystals aligned parallel to the surface normal. In the blended films, two types of crystals (PVDF-TrFE and PVDF-TrFE-CTFE) were independently formed on the oriented P3HT crystals (Supporting Information, Figure S3). For instance, a 2D GIWAXS pattern of a 10:5 blended film of Figure 1c displayed two intensified reflections of both PVDF-TrFE and PVDF-TrFE-CTFE crystals. The two independent types of crystalline reflections developed in the mixture of the PVDF-TrFE-CTFE and PVDF-TrFE indicate that the two polymers were apparently phase-segregated with each other, and formed their own crystals at room temperature. In addition, both morphology and diffraction results clearly show that the edge-on microdomains of both PVDF-TrFE and PVDF-TrFE-CTFE crystals with their *c*-axis aligned parallel to the surface were well developed on the oriented P3HT crystals in our Fe-FET device. The preferred orientations of both ferroelectric crystals and P3HT are beneficial for facile polarization switching of H–F dipoles under an electric field as well as efficient inter-chain charge transport in a Fe-FET,.[22,28]

Thin uniform film formation of PVDF-TrFE and PVDF-TrFE-CTFE blends after thermal annealing at 135 °C was examined by root mean square (RMS) roughness measured using atomic force microscopy (AFM), as plotted in **Figure 2**a. The surface topography and phase images of various PVDF-TrFE/PVDF-TrFE-CTFE blend films (Supporting Information, Figure S4) clearly show that the blended films were all very smooth, with surface RMS roughness ranging from 1.9 to 3.5 nm. These roughness values are comparable to the roughness of a pure PVDF-TrFE film of approximately 4.2 nm, which implies that our blended films are all suitable for thin film ferroelectric memory applications.

Further, simple solution blending of the two polymers provides a convenient way for controlling film capacitance. Figure 2b shows the dielectric constant values determined from capacitance–voltage (*C*–*V*) measurements of Au/blended ferroelectric layer (3.5 wt%)/highly doped Si (metal/ferroelectric/metal: MFM) capacitors with different blending ratios. *C*–*V* curves of MFM capacitors all exhibited characteristic butterfly shapes upon voltage sweep, which arose from ferroelectric dipole switching in the films (Supporting Information, Figure S5). The dielectric constants of the films were calculated from the capacitance values of MFM capacitors at 0 V. The

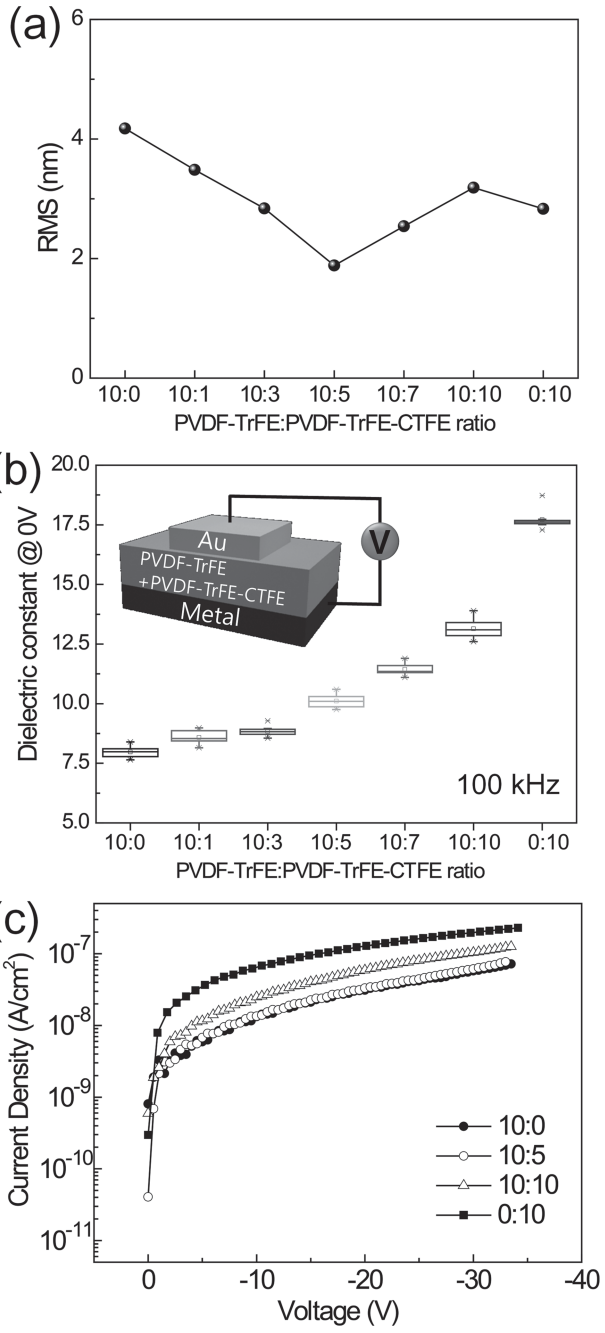

Figure 2. a) The average surface RMS roughness of ferroelectric gate insulator layers with different blending compositions. b) Dielectric constant calculated from the capacitance values from capacitance–voltage measurements at V = 0, and c) leakage current density of Au/ferroelectric blended layer (3.5 wt%)/highly doped Si capacitors with different blending compositions.

dielectric constants were systematically controlled by blending PVDF-TrFE ($k \approx 8$) and PVDF-TrFE-CTFE ($k \approx 18$) with different blend compositions. A very narrow variation of the dielectric constant, represented by box-whisker plots in Figure 2b, further supports the facile control of the electrical properties by solution blending.

It is also very important to make the leakage current of a blended film as low as possible while maintaining a high capacitance. The low leakage current ensures a low OFF state current (I_{DS}) in a FeFET, which can give rise to an MLC device with clearly distinguishable current levels. Current–voltage (I–V) characteristics of MFM capacitors with blend compositions of PVDF-TrFE and PVDF-TrFE-CTFE from 10:1 to 10:10 showed a leakage current at a low level (<10^{-7} A cm^{-2}) when the bias voltage was less than 30 V, as shown in Figure 2c. The leakage current level did not change significantly with PVDF-TrFE-CTFE and in particular, a blended film of 10:5 mixing composition with which we characterized all the multi-level non-volatile memory performances as shown later has a leakage current level very similar to that of a neat PVDF-TrFE film (also See Supporting information, Figure S6). These levels of leakage current are much lower than those of the hybrid films containing inorganic high-k materials such as $BaTiO_3$, in which leakage current mainly arises from trap-assisted tunneling.[29] Our blended film, which had a low leakage current as well as high capacitance, can be advantageous for low voltage operating MLC FeFETs as long as the ferroelectric properties of the film are guaranteed.

Figure 3a,b shows the values of remnant polarization (P_r) measured from polarization versus voltage hysteresis loops of MFM capacitors containing various blended films when the sweep voltage was applied to capacitors of ±60 and ±30 V (see Supporting information, Figure S7). For a large sweep voltage of ±60V, the hysteresis loop of an MFM having a ≈350-nm-thick PVDF-TrFE film was nearly saturated with a P_r of approximately 6.4 μC cm^{-2} and a coercive field of approximately 65 MV m^{-1}. Both coercive field and P_r value observed were quite consistent with the values of a previous study by Zhang and co-workers.[30] As the amount of PVDF-TrFE-CTFE in the blended films increased to a 10:10 blend composition, the P_r values slightly decreased because of the relaxer characteristics of pure PVDF-TrFE-CTFE, which has a near-zero hysteresis, as shown in Figure 3a. It should be noted that the asymmetric P–V hysteresis curve in Figure S7, Supporting Information, arises from asymmetric electric contact of a ferroelectric polymer with the top and bottom electrodes. The work by Zhang and co-workers[30] well demonstrated that top and bottom electrodes with different work functions gave rise to asymmetric coercive voltage upon voltage sweep. They found that the asymmetric phenomena were mainly ascribed to the different Schottky emission and charge injection at the interface of a PVDF-TrFE with different metal electrode. In our system, asymmetric hysteresis also results from different top and bottom electrodes: highly doped Si and Au, respectively.

When the capacitors were swept with a low voltage of ±30 V, below which a FeFET device could be regarded as capable of low voltage operation, a partially saturated ferroelectric polarization of approximately 2.4 μC cm^{-2} was obtained with a pure PVDF-TrFE. The value was not significantly altered with PVDF-TrFE-CTFE, as shown in Figure 3b. The results clearly suggest that high capacitance arising from PVDF-TrFE-CTFE in a blended film could lead to low voltage operation of a ferroelectric memory device since the surface charge density of approximately 2.0 μC cm^{-2} on a ferroelectric layer is sufficient to fully accumulate hole carriers of various organic

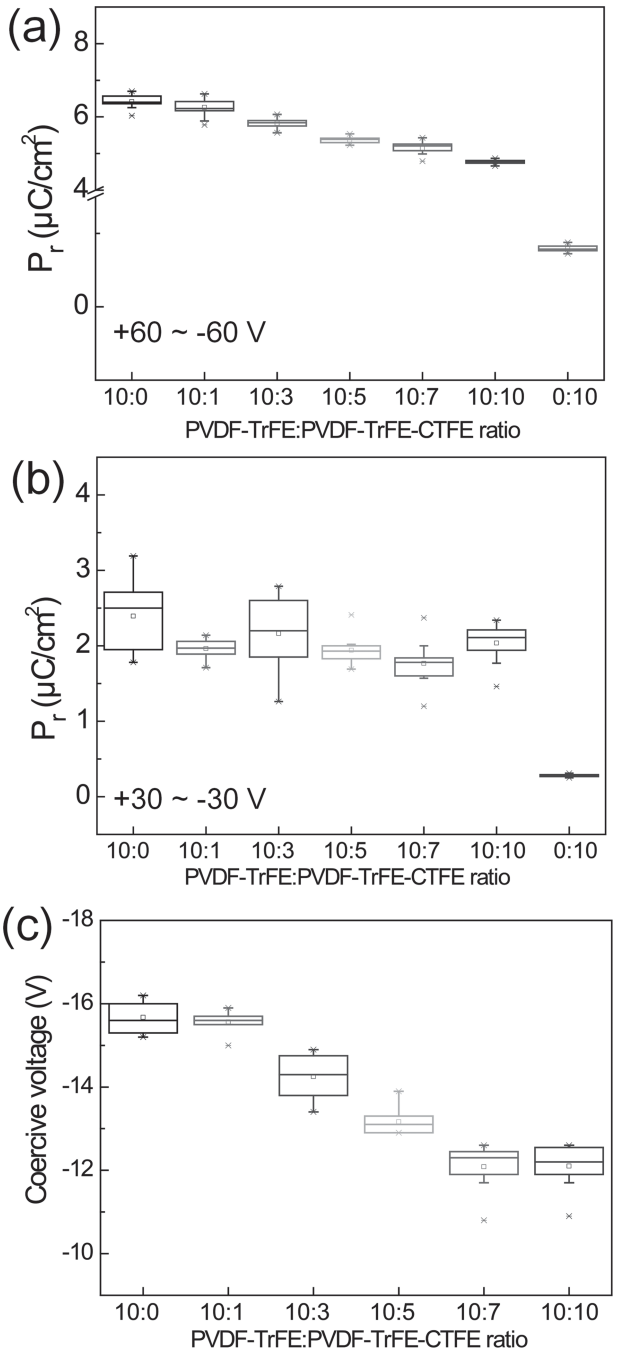

Figure 3. The box-whisker plots of the distribution of remanent polarization (P_r) at a) ±60 V and b) ±30 V DC sweep conditions, and c) coercive voltage measured from polarization vs. voltage hysteresis loops of capacitors obtained with a voltage sweep of ±30 V.

semiconductors such as pentacene,[31,32] MEH-PPV,[10] and P3HT[16] at the channel, giving rise to a saturated I_{DS} hysteresis curve. As expected, the minimum voltage for ferroelectric switching, that is, the coercive voltage, decreased with the amount of PVDF-TrFE-CTFE due to a reduction in equivalent ferroelectric thickness (EFT) by increasing the dielectric constant, as shown in Figure 3c. More detailed characteristics of

Table 1. Characteristics of MFM and Fe-FET devices with ferroelectric insulators as a function of the blending ratio of PVDF-TrFE/PVDF-TrFE-CTFE.

			MFM Capacitor					Transistor
Blending ratio	Thickness [nm]	RMS [nm]	k[a)]	EFT[b)] [nm]	Leakage Current [$\times 10^{-8}$ A cm^{-2}]	P_r[c)] [μC cm^{-2}]	Coercive Voltage[c)] [V]	On-off ratio[e)]
10:0	340	4.2	8.0	340	5.2	2.4	15.7	10^1–10^2
10:1	346	3.5	8.6	322	4.6	2.0	15.6	10^1–10^2
10:3	340	2.8	8.8	309	5.1	2.2	14.2	10^2
10:5	366	1.9	10.1	290	5.4	1.9	13.1	10^3–10^4
10:7	346	2.5	11.4	243	8.9	1.8	12.1	10^3–10^4
10:10	342	3.2	13.1	209	9.7	2.0	12.1	10^2–10^3
0:10	332	2.8	17.7	150	19.5	0.3	–[d)]	10^1

[a)]Measured from C–V curves; [b)]Equivalent ferroelectric thickness (EFT) was calculated as thickness × (pure PVDF-TrFE k/blending material k); [c)]Measured from P–V hysteresis loops at +30 to −30 V, DC sweep condition; [d)]Value is negligible (no hysteresis loop); [e)]Calculated from I_{DS}–V_G transfer curves at V_G 0 V.

MFM capacitors with the blended ferroelectric films are also summarized in **Table 1**.

Fe-FET devices containing PVDF-TrFE, PVDF-TrFE-CTFE, and a blended film (10:5) all exhibited p-type transfer characteristics in the source-drain current (I_{DS}) versus gate voltage (V_G) at a V_{DS} of −5 V, as shown in **Figure 4**a. In addition, current hysteresis is apparent, which resulted from the ferroelectric polarization switching of a gate insulator. When a negative gate voltage was applied, there was a rapid increase in I_{DS} owing to accumulation of excess holes in the P3HT layer. When the V_G returned to zero, the I_{DS} remained saturated due to the nonvolatile H–F dipoles, with the fluorine atoms pointing to the P3HT layer. The subsequent application of a positive V_G on the device gradually switched the H–F dipoles, leading to a decrease in the I_{DS}. A hysteresis with a very small ON-OFF ratio at 0 V was obtained with a PVDF-TrFE-CTFE insulator due to the small P_r value (approximately 0.3 μC cm^{-2}) in its MFM capacitor. Interestingly, a fully saturated hysteresis curve was achieved in a device containing the 10:5 blended film with an ON-OFF ratio greater than 10^4 at a V_G of ±30 V, while a Fe-FET with a PVDF-TrFE insulator was not saturated with a relatively small ON-OFF ratio of approximately 10^2, as shown in Figure 4a.

As clearly shown in Figure 4b, as the amount of PVDF-TrFE-CTFE in blended films increased, the hysteresis curves were gradually saturated, as evidenced by the lowering OFF-current. When the V_G sweep from +30 V to 0 V, the nonvolatile H–F dipoles of PVDF-TrFE were switched from the fluorine atoms pointing to P3HT layer to the hydrogen atoms pointing to the P3HT layer, leading to the decrease of the I_{DS} which arose from depletion of holes in the P3HT channel. A Fe-FET with a neat PVDF-TrFE exhibited a partially saturated current hysteresis curve at the gate voltage sweep of ±30 V due to the high coercive voltage of the PVDF-TrFE film. This incomplete ferroelectric domain switching from +30 V to 0 V again rendered P3HT layer incompletely depleted, leading to relatively high OFF current level. The device with the PVDF-TrFE film was finally saturated at a V_G of ±40 V (Supporting Information, Figure S8). On the other hand, a device containing a blended ferroelectric insulator with low coercive voltage showed a fully saturated hysteresis curve with low OFF current level which resulted from completely depleted P3HT layer as shown in Figure 4a. When the amount of PVDF-TrFE-CTFE increased further, gate leakage became dominant, giving rise to high OFF current as evidenced in Figure 3b. In our experimental conditions, the maximum ON/OFF ratio was obtained with 10:5 and 10:7 blended samples. In consequence, the best memory performance with a high ON-OFF ratio for MLC operation was observed in a Fe-FET containing a 10:5 blended film, as shown later.

The variation in ON current at 0 V as a function of programmed gate voltage of $0 \rightarrow V_G \rightarrow 0$, shown in Figure 4c, clearly shows that the ON current with a blended insulator increased more rapidly with the programmed V_G. This implies that the blended film can significantly reduce the operating voltage as compared to the pure PVDF-TrFE. A similar ON current behavior with the programmed V_G was also observed with other blended insulators, supporting the role of PVDF-TrFE-CTFE as a high-k additive (Supporting Information, Figure S9).

To realize a low operating voltage in a MLC Fe-FET with our blended insulator, we optimized the amount of PVDF-TrFE-CTFE as well as film thickness and fabricated a Fe-FET with a blended (10:5) ferroelectric film spin-coated from a solution (polymer concentration of 2.5 wt%). For this purpose, first, the minimum film thickness of a neat PVDF-TrFE film which exhibited reliable Fe-FET performance was determined before adding PVDF-TrFE-CTFE for lowering operation voltage. Approximately 250 nm thick film showed reliable Fe-FET performance, below which a device was very leaky. Based on this condition, we optimized multi-level device performance with PVDF-TrFE-CTFE. The Fe-FET device exhibited a fully saturated I_{DS} hysteresis with a very low gate voltage sweep of ±18 V, while a device with a neat 250 nm thick PVDF-TrFE insulator exhibited a fully saturated I_{DS} hysteresis with a gate voltage sweep of ±25 V, as shown in Supporting information, Figure S10. Approximately 40% decrease of the operation voltage was obtained due to the reduction of effective ferroelectric thickness (EFT).

Next, multilevel data storage of the I_{DS} with continuous and distributed ferroelectric domain switching of a ferroelectric blended insulator was investigated as a function of gate

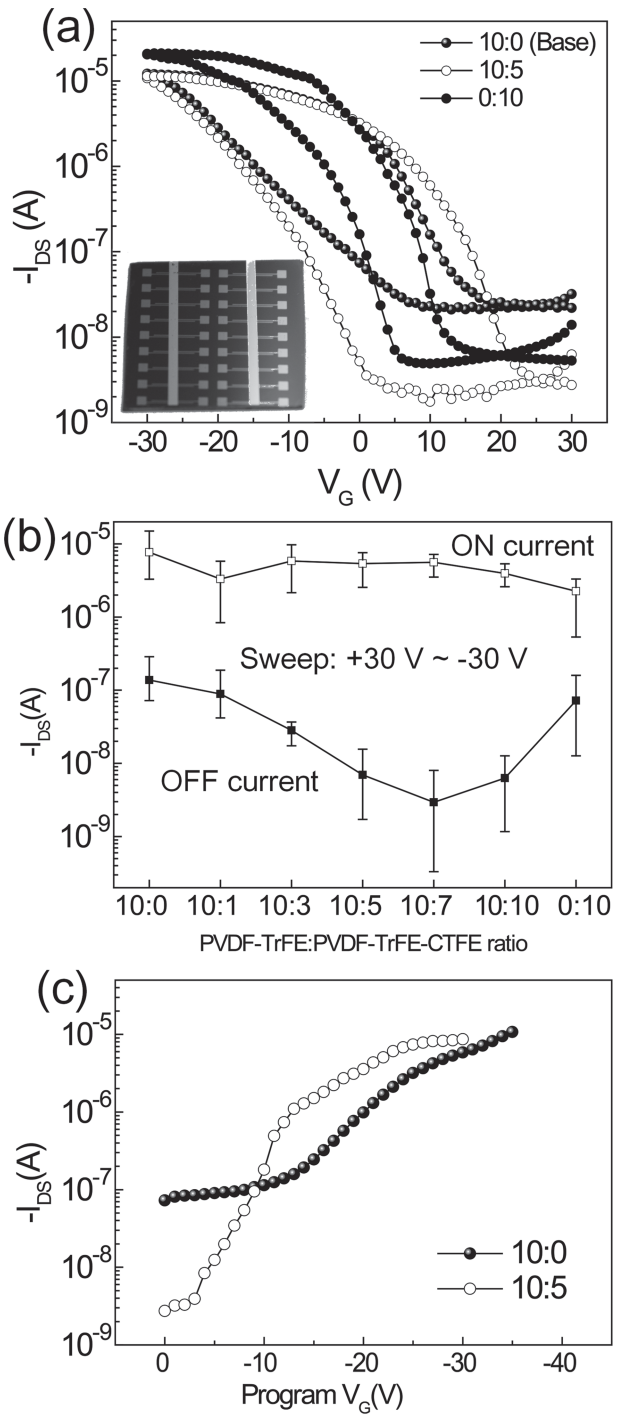

Figure 4. a) I_{DS}–V_G transfer curves and b) ON/OFF current values of Fe-FET devices with various blended insulators measured at a read voltage (V_G = 0 V). c) I_{DS} values of Fe-FET devices containing a neat PVDF-TrFE and a blended insulator obtained at a read voltage after various program V_G values ranging from –0 to –35 V in the DC sweep mode.

voltage, and the results are shown in **Figure 5**a. First, the OFF state (erase state, ERS) in the Fe-FET was set up with a V_G of +18 V in DC sweep mode. The plot of I_{DS} values measured at V_G = 0 V after various DC sweep V_G steps in Figure 5a shows that non-volatile current states almost linearly increased in log scale when the program gate voltage sweep was between –7 and –15 V due to pseudo-continuous ferroelectric domain switching of the blended insulator.[15] Within the regions, several interstates (IRSs) can be assigned with distinguishable current separation, as indicated in Figure 5a. At a high gate voltage sweep above –15 V, the I_{DS} at V_G = 0 V did not change significantly due to saturation of the channel. The results suggest that multilevel operation of a cell can be achievable at such a low operating voltage as long as the programming V_G is precisely controlled with a sufficient reading margin of the I_{DS} at V_G = 0 V between two IRSs.

We successfully demonstrated a six-level MLC Fe-FET in which four IRSs were chosen with program voltages of –9, –11, –13, and –15 V, in addition to complete erase and saturated program states (ERS and PGM) at +18 and –18 V, respectively. After complete erase at V_G = +18 V, the lowest current OFF state was set as the ERS, as shown in Figure 5a,b. The subsequent independent gate voltage sweep at ±9, ±11, ±13, and ±15 V resulted in 4 different I_{DS} hysteresis curves, with which we were able to define four interstates of IRS-1/IRS-2/IRS-3/IRS-4 at V_G = 0. Finally, a full sweep of the device at ±18 V developed a saturated I_{DS} hysteresis curve, and the sixth level PGM was determined at V_G = 0, as shown in Figure 5b.

The device reliability of our six-level MLC Fe-FET with a blended insulator was investigated by both time-dependent data retention and multiple data writing/erasing endurance. Data retention was examined by independently measuring six non-volatile I_{DS} values set by different gate voltage sweeps at V_G = 0 V with a constant V_{DS} of –5 V, as described in detail in our previous report.[15] Figure 5c shows highly reliable data retention of all six levels for up to about 10^4 s. Most inorganic Fe-FETs suffer from poor data retention due to a severe depolarization field by charge injection from the semi-conducting channel into the ferroelectric layer due to low band gap energies of the inorganic ferroelectrics.[33] Although charge injection rarely occurred due to the high energy band gap of most ferroelectric polymers in organic Fe-FETs, the depolarization field was caused by the field-effect band bending in the semiconductor.[34] In particular, the field-effect band bending becomes severe with a decrease in the thickness of a ferroelectric layer, making it very difficult to fabricate an organic Fe-FET with a very thin ferroelectric polymer insulator operating at low voltage.

In the case of a ferroelectric capacitor with a dielectric interlayer, the depolarization field becomes more completed. The equation shown in Supporting information, Figure S11,[35,36] suggests that the depolarization field would increase with total polarization of a device and decrease with dielectric constant of a ferroelectric layer. In our field effect transistor memory, the polarization of a ferroelectric insulator should be balanced with the maximum amount of charges accumulated for saturation of a P3HT channel. In fact, approximately 2 μC cm^{-2} was required to saturate source-drain current in Fe-FET memories with organic semiconductors, as explained previously. In this circumstance, the total polarization value of our blended films with different compositions is assumed to be all similar. Since the dielectric constant of a blended film increases with the amount of PVDF-TrFE-CTFE, the depolarization field would,

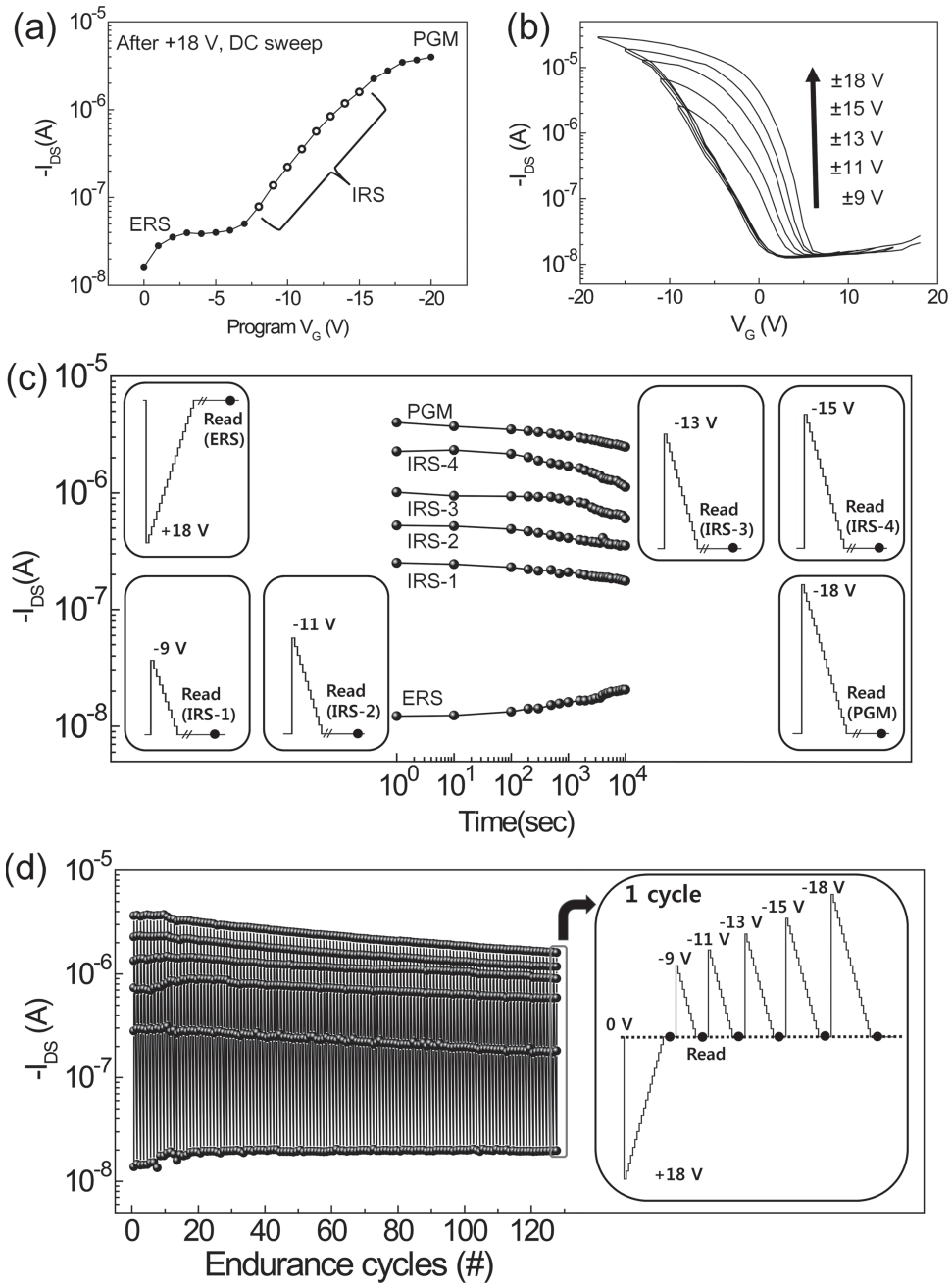

Figure 5. a) Non-volatile I_{DS} values of the Fe-FET with the ferroelectric blended insulator (10:5, 2.5 wt%) obtained at a read voltage (V_G = 0 V) after various program V_G values ranging from 0 to −18 V in the DC sweep mode. Six distinct I_{DS} values at appropriate program voltages highlighted in (a) were used for the six-level Fe-FET. b) The multilevel I_{DS}–V_G transfer curves of a Fe-FET after various program V_G values. c) The time-dependent retention characteristics and d) multiple write/erase endurance cycles of multilevel I_{DS} values established in a Fe-FET. The insets in (c) and (d) show the test sequence applied in the DC sweep mode for the multilevel retention and endurance measurements, respectively.

therefore, decrease with the PVDF-TrFE-CTFE, which would be additionally beneficial for long term reliability of a device with a blended film. In fact, a recent simulation work also revealed that long term data retention property was enhanced with a memory device having high-*k* ferroelectric layer, compared with one containing low-*k* ferroelectric layer.[37] Our approach for lowering operating voltage by reducing EFT with a high-*k* polymer while maintaining a sufficiently thick ferroelectric layer can avoid severe depolarization, giving rise to highly reliable data retention for all six different states.

For multiple data write/erase endurance cycling tests, we consecutively measured six-level non-volatile I_{DS} values with the programmed endurance cycle. The sequence used was erase/read/program-1/read/program-2/read/program-3/read/program-4/read/program-5/read/program-6/read, with six corresponding DC program gate sweeps of +18 to 0 V,

–9 to 0 V, –11 to 0 V, –13 to 0 V, –15 to 0 V, and –18 to 0 V, respectively, as shown in the schematic of Figure 5d. Highly reliable and reproducible six-level cycles were achieved over 120 cycles, as shown in Figure 5d. Both high performance data retention and endurance cycles of our six-level Fe-FET memory at low operating voltage of ±18 V are indeed notable, considering that most floating gate and resistive types of multilevel organic memories show long data retention but often unstable multilevel switching endurance due to the degradation of the tunneling layer or conducting filament under repeated program/erase cycles.[38–43] In this sense, our MLC Fe-FET memory is advantageous because it is based not only on nondestructive write/read operation by a semiconductor, but also on polarization switching, which is electrically much more stable than conduction switching. It should be also noted that the current levels of intermediate states in our Fe-FET were selected arbitrarily as long as they were readily distinguished with each other even after long time retention, and repeatedly and consistently addressed at constant programming and reading gate voltages. As shown in Figure 5d, the current level of each intermediate state hardly changed upon write-read cycle test.

Although the operating voltage of a ferroelectric polymer based FET is in principle scaled linearly down with the decrease of the film thickness due to the constant coercive field of a PVDF-TrFE of approximately 50 MV m^{-1}, the operation of a device with a PVDF-TrFE film lower than 100 nm in thickness is considered extremely difficult because of the many structural defects and large surface roughness of the film. Our approach is different from other previous works for reducing operation voltage of Fe-FETs, for instance, using nanoconfinement of ferroelectric crystals in the self assembled inorganic nanopatterned surface and dense and thin ferroelectric films based on proper selection of solvents. Most of the works including our previous work are, however, conducted for conventional bi-state, 1 bit non-volatile memory devices. For multi-state Fe-FETs, two critical properties should be additionally satisfied of 1) large ON and OFF current margin for assigning discrete intermediate states and 2) high reliability of each intermediate state in terms of data retention with time and write-read cycle endurance.

As noted, at most ON/OFF ratio of approximately 100 was demonstrated with low-voltage operating devices in the previous cases. In general, the lower the operating voltage of a device, the smaller ON/OFF ratio was obtained mainly due to gate leakage from a thin PVDF-TrFE layer which resulted in high OFF current.[34,44] This small ON/OFF ratio certainly makes it difficult to discretely write and read the intermediate states. Furthermore, although the previous studies showed current hysteresis curves obtained at a few gate voltage sweep with partially saturated ferroelectric domains, no reliability test was performed. We do believe that the reliability of those partially saturated hysteresis curves would be very poor, mainly because of depolarization field imposed on the ferroelectric film.[33] In fact, we fabricated a Fe-FET device with a neat PVDF-TrFE (<100 nm) prepared from 1 wt% polymer solution and observed a characteristic ferroelectric hysteresis loop operating at the gate voltage sweep of ±10 V, as shown in Supporting information, Figure S11. The device, however, exhibited high gate leakage current, making its ON/OFF ratio of approximately 10 with very poor device yield less than 10%. ON current data retention results showed that high current level through P3HT channel at the accumulation state was properly held by non-volatile ferroelectric polarization at the beginning but it gradually decreased with time due to the depolarization field and reached at a current level very close to the OFF current one.

Our approach of blending high-*k* polymer with ferroelectric one resolved these issues. In addition to low voltage operation of a Fe-FET with high capacitance of a blended ferroelectric gate insulator, physically thick ferroelectric layer of approximately 250 nm in thickness not only significantly reduced gate leakage current, guaranteeing high ON/OFF ratio, but also minimized depolarization field, giving rise to reliable multi-state operation as clearly demonstrated in Figure 5. It should be also noted that compared with the previous bi-state Fe-FETs having reliable data retention and endurance, our results clearly show that only ±9 V was sufficient for reliable bi-state data storage.

It should be also mentioned that although the concept is different, we have already reported low-voltage operation of bi-state, 1 bit Fe-FET devices based on a solution blend of ferroelectric polymers with amorphous PMMA. In the previous work,[2] PMMA was, however, blended with not PVDF-TrFE but PVDF to preferentially develop ferroelectric crystals upon competition between paraelectric alpha phase and ferroelectric beta one. Thin smooth blended film additionally allowed low voltage operation of a bi-state Fe-FET at the gate voltage sweep of ±15 V. In the other work,[45] we blended PVDF-TrFE with PMMA mainly in order to characterize molecular and microstructures of ferroelectric films as a function of PMMA.

Switching characteristics of our MLC-FeFETs are also important. Although intrinsic switching of a PVDF-TrFE occurred in approximately a few nanosecond level, its switching speed was varied, depending on the types of devices.[46] For instance, metal/ferroelectric/metal capacitors showed in general switching time of an order of microseconds while field effect transistor type devices exhibited switching time of 10^{-3} to 10^{-4} s.[47–49] Since frequency dependent dielectric behavior of PVDF-TrFE-CTFE is very similar to that of PVDF-TrFE,[50] low device operation with a blended film would be also made at high frequency regime of 1 MHz. In addition, we believe our device with the high-*k* blended ferroelectric film can show better switching speed characteristics than those with a neat PVDF-TrFE film, owing to lower coercive voltage by high capacitance.

3. Conclusions

We demonstrated a high performance non-volatile multilevel polymer Fe-FET memory operating at a low voltage. The precise control of the capacitance of a ferroelectric gate insulator layer was the key development for low voltage operation of the device by solution-blending a ferroelectric polymer (PVDF-TrFE) with high-*k* polymer (PVDF-TrFE-CTFE). A thin uniform blended film with high capacitance as well as low leakage current gave rise to a fully saturated current hysteresis with a large ON-OFF current margin, ensuring multilevel data storage at low driving voltage due to the facile reduction of effective ferroelectric

thickness of the insulator. At optimized conditions, our MCL Fe-FET with a blended insulator showed discrete six-level multi-state operation at a gate voltage sweep of ±18 V, with excellent data retention and endurance of each state of more than 10^4 s and 120 cycles, respectively. Our results provide a novel design strategy for ultra high-density non-volatile polymer memory operating at low power.

4. Experimental Section

Materials and Film Preparation: PVDF-TrFE with 25 wt% TrFE was purchased from MSI Sensors. PVDF-TrFE-CTFE with its monomer ratio of 66:34:8.3 was provided by Samsung Electronics Co. Ltd. P3HT (M_w = 180 000 g mol^{-1} with 98.5% head to tail regioregularity) was purchased from Sigma Aldrich, Korea. All organic solvents including methyl ethyl ketone (MEK) and 1,2-dichlorobenzne (DCB) were purchased from Sigma Aldrich, Korea. A P3HT solution in DCB (1 wt%) was spin-coated at 2000 rpm for 70 s on a SiO_2 (500 nm) substrate with patterned Au S/D electrodes. The spin-coated P3HT films were dried under vacuum for 2 h at 60 °C. PVDF-TrFE/PVDF-TrFE-CTFE blending solution in MEK with various blending ratios was spin-coated at 1500 rpm for 60 s on a P3HT layer. The spin-coated films were annealed for 2 h at 135 °C.

Capacitor Fabrication and Characterization: Metal/ferroelectric blend films/metal capacitors were made with a highly boron-doped Si substrate as the bottom electrode. Au top electrodes were thermally evaporated on ferroelectric films using a shadow mask with squares of 400 μm × 400 μm under a vacuum of 10^{-6} Torr (SNTEK MEP5000). Ferroelectric polarization–voltage measurements were performed using a virtual ground circuit (Radiant Technologies Precision LC unit). *C–V* and *I–V* characteristics were measured using an Agilent Technologies E5270 DC analyzer and an Agilent 4284A precision LCR meter at a frequency of 100 KHz under ambient conditions. The thickness of ferroelectric films was measured using an Alpha step 500 Surface Profiler (AS500) (KLA-Tencor Co.).

Fe-FET Fabrication and Characterization: SiO_2 substrates were cleaned in an ultrasonic bath with acetone and ethanol for one hour each. First, arrays of 30-nm-thick Au S/D electrodes were thermally evaporated on a substrate with a patterned shadow mask under a vacuum of 10^{-6} Torr. Subsequently, an approximately 50-nm-thick P3HT layer was spin-coated. After thermal treatment at 60 °C for 2 h to remove the residual solvents in the P3HT, the blended ferroelectric insulators were spin-coated on a P3HT layer. The PVDF-TrFE solution in MEK did not affect the underlying P3HT layer. The blend films were annealed at 135 °C on a heating stage (Linkam 600, UK) for 2 h. The 70-nm-thick top gate Al electrodes were deposited by thermal evaporation under a vacuum of 10^{-6} Torr with a patterned shadow mask aligned with respect to the S/D electrodes previously formed. In order to make the Au S/D electrode accessible with contact probe tips, the devices were further treated with oxygen plasma (100 W for 200 s, 10^{-3} Torr, 40 sccm) generated by reactive ion etching (RIE) (Femto VITA-4E). Arrays of Al gate electrodes were used as RIE blocking masks, giving rise to top-gate-bottom-contact Fe-FET memories with S/D electrodes open to the air, as illustrated in the schematic in Figure 1a. The electrical characteristics were measured using a semiconductor system (E5270B, Agilent Technologies) under ambient conditions.

Structure Characterization: The structure of the films was characterized using field emission scanning electron microscopy (FESEM, LEO 1550 VP), AFM (Nanoscope IV a Digital Instruments) in tapping mode, and by two-dimensional (2D) grazing-incidence wide-angle X-ray scattering (GIWAXS). The latter experiments were performed on the 9A beam line at the Pohang Accelerator Laboratory in Korea (incidence angle: 0.09°–0.15°). The samples were mounted on an *x*- and *y*-axes goniometer. The scattered beam intensity was recorded with an SCX: 4300-165/2 CCD detector (Princeton Instruments). 2D GIWAXS patterns were obtained in the range $0 < q_z < 2.33$ Å^{-1}, $0 < q_{xy} < 2.33$ Å^{-1}. An optical microscope (OM) was used to visualize the Fe-FET devices (Olympus BX 51M).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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